HK32F030x4/HK32F030x6/HK32F030x8

data sheet

Rev0.7

targetrecord

History

Version	Date	Description
1.0.0	2018/06/08	initial version
1.0.1~1.0.6		internal version
1.0.7	2019/06/10	correctflash programThe number of times is1K

1 illustrate

Shenzhen Hangshun Chip Technology Research Co., Ltd. is based onARM Cortex-M0Developed and designedHK32F030, HK32F031,HK32F03XThree series of chips, collectively referred to asHK32F03xproduct line.

This document isHK32F030x4/HK32F030x6/HK32F030x8Chip data sheet.HK32F030The series chips are low power consumption developed by Shenzhen Haohan Skyline Processor Co., Ltd., a subsidiary of Shenzhen Hangshun Chip Technology Research Co., Ltd.MCUchip, please contact Shenzhen Haohan Skyline Processor Co., Ltd. to provide more related documents.

2 Product Overview

2.1 Features

- Operating voltage range

  -Single Power Domain: Main PowerVDD 2.0V ~ 5.5V

- Typical operating current
  - Dynamic power consumption:120uA/MHz
  - StopStandby power consumption:10uA@3.3V
  - StandbyStandby power consumption:1.6uA@3.3V
- range of working temperature:-40ºC ~ 105ºC
- Chip clock source
  - externalHSE:support4~16MHzcrystal, typical8MHzCrystal external
  - LSE:32.768KHzcrystal oscillator
  - on-chipRCOscillator Clock:8MHz/14MHz/56MHz
  - Configurable on-chipLSIclock:40KHz PLLclock
  -
  - Chip pin input clock

-Chip internal system clock source

- All clock sources of the chip can be selected as system clocks, including slow clocksLSIandLSE. The user has the flexibility to select the system clock according to the power consumption and performance requirements of the application.

-reset

- External pin reset
- Power on reset
- software reset
- watchdog (IWDTandWWDT) timer reset low
- power mode reset

- Low voltage detection (PVD)
  - 8Stage detection voltage threshold adjustable
  - Rising and falling edge configurable
- ARM Cortex-M0 Core
  - Maximum clock frequency:72MHz
  - twenty fourbitSystem Ticktimer
  - supportCPU Eventsignal input toMCUpins, implemented with other board-levelSOC CPUlinkage

-memory

- Gundam64KByteofFlashmemory.CPUfrequency not higher than24MHz, support0Wait for a bus cycle. With code security protection function, read protection and write protection can be set separately; can be encryptedFlash instructions and data stored on theFlashContent is physically attacked. Gundam10KByte
- SRAM,noHW ParityFunction

-One12bitSAR ADCconverter

- Gundam16External analog signal input channels
- Maximum Converter Frequency:1Mbps
- Support automatic continuous conversion, scan conversion

- Temperature Sensor

-The analog output is internally connected toA/DConverter independent channel

- debug interface

-SWDdebug port

- Universal Serial Communication Interface

- Gundam2indivualUSART, supports master syncSPIand modem control, withISO7816interface, LIN,IrDA Capability auto-baud rate detection and wake-up feature
- Gundam2high speedSPI,have4to16programmable bit frames, multiplexedI^2SInterface up to2
- indivualI2C, supports extreme speed mode (1 Mbit/s) ,SMBus/PMBus, can be called from stop mode Awake

-timer

- TIM1Advanced control timer, with6aislePWMoutput, as well as deadband generation and emergency stop
- functions TIM3/TIM14/TIM15/TIM16/TIM17General purpose timer TIM6basic timer
-

-General purpose input and outputIO

- Gundam55indivualGPIOpin
- allGPIOPin Configurable as External Interrupt Input
- provide the highest20mAdrive current

- five channelDMAcontroller, supportTimers,ADC,SPIs,I2Cs,USARTsand other peripheral triggers
- CRCcalculation module
- Fixed-point division/square root unit

- support32Fixed-point division with quotient and remainder at the same time
- support32High-precision square root of fixed-point number

- calendarRTC, with alarm to wake up from stop/standby cycle
- reliability

-pass throughHBM2000V/CDM500V/MM200V/LULevel test

2.2 Device overview

Peripherals	HK32F030
package	LQFP64/LQFP48/LQFP32/TSSOP20
Dynamic power consumption	120uA/MHz
Power consumption	Sleep:60uA/MHz STOP:10.5uA Standby:1.6uA with 100us wakeup time
clock source	32KHz OSC 32MHz OSC 40KHz RC 56MHz RC PLL
System reset	POR PDR External RST IWDG WWDG Soft-Reset
Analog peripherals	16aisleADC Temperature Sensor PVD
CPUmain frequency	maximum72MHz
VDDOperating Voltage	2.0~5.5V
VBATinput pin	without
Flash (KBytes)	64
SRAM(KBytes)	10
DMA	5aisle
FSMC	without
timer	TIM1/TIM3/TIM6/TIM14/TIM15/TIM16/TIM17
SPI/I2S	2
IIC	2
USART	2
USB	without

CAN	without
SDIO	without
DIVSQRT	1

2.3 order code

specific model	Package	Minimum package quantity
HK32F030R8T6	tape orTrayplate	
HK32F030C8T6	tape orTrayplate	
HK32F030C6T6	tape orTrayplate	
HK32F030K6T6	tape orTrayplate	
HK32F030F4P6	tape orTrayplate	

The naming rules are as follows:

Example: HK32 F 030 C 6 T 6 x

Device family

HK32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

030 = HK32F030

Pin count

F = 20 pins
K = 32 pins
C = 48 pins
R = 64 pins

Code size

4 = 16 Kbyte of Flash memory
6 = 32 Kbyte of Flash memory
8 = 64 Kbyte of Flash memory
C = 256 Kbyte of Flash memory

Package

P = TSSOP
T = LQFP

Temperature range

6 = –40 to 85 °C

Options

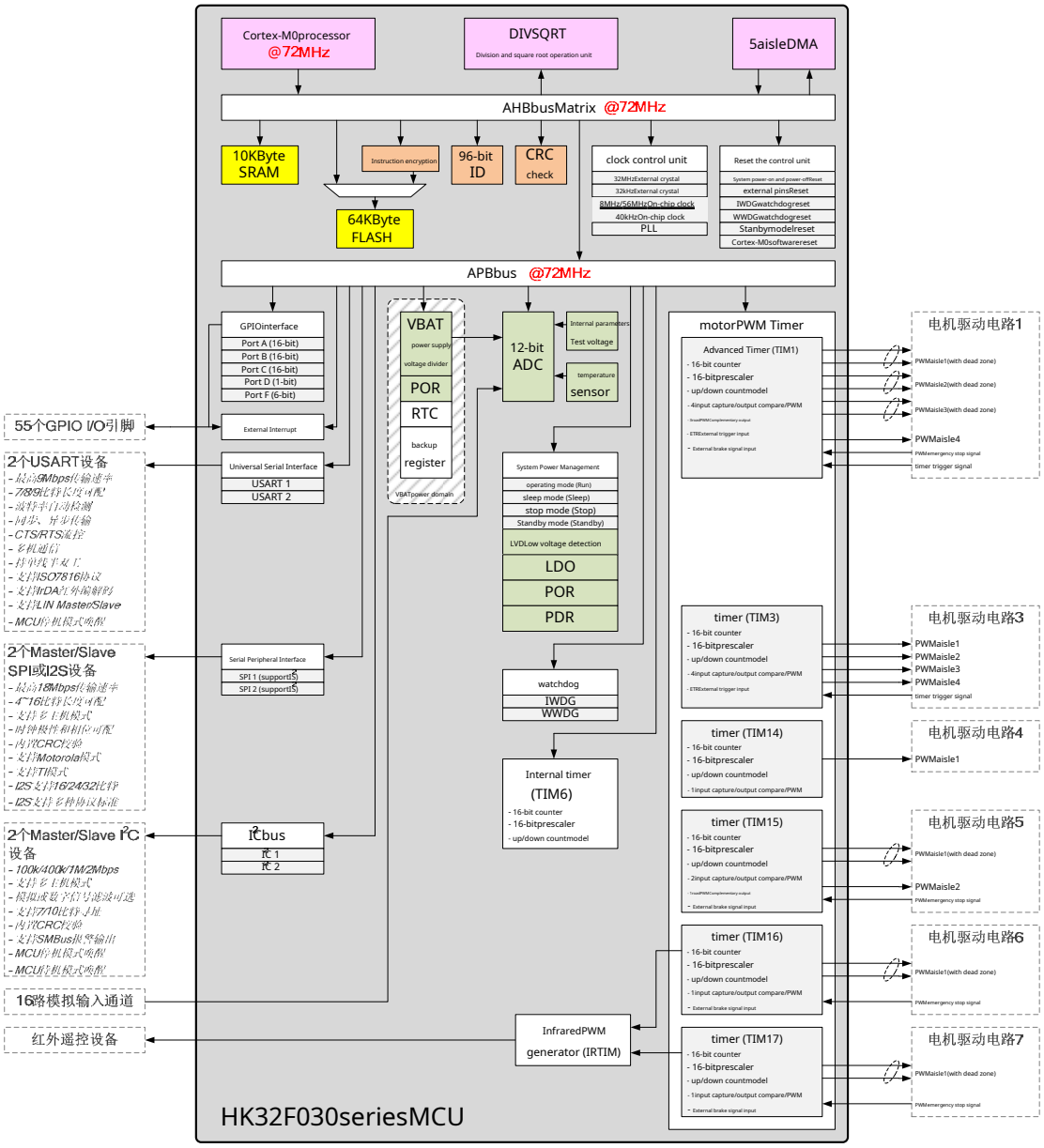
xxx = programmed parts
TR = tape and reel

3 Features

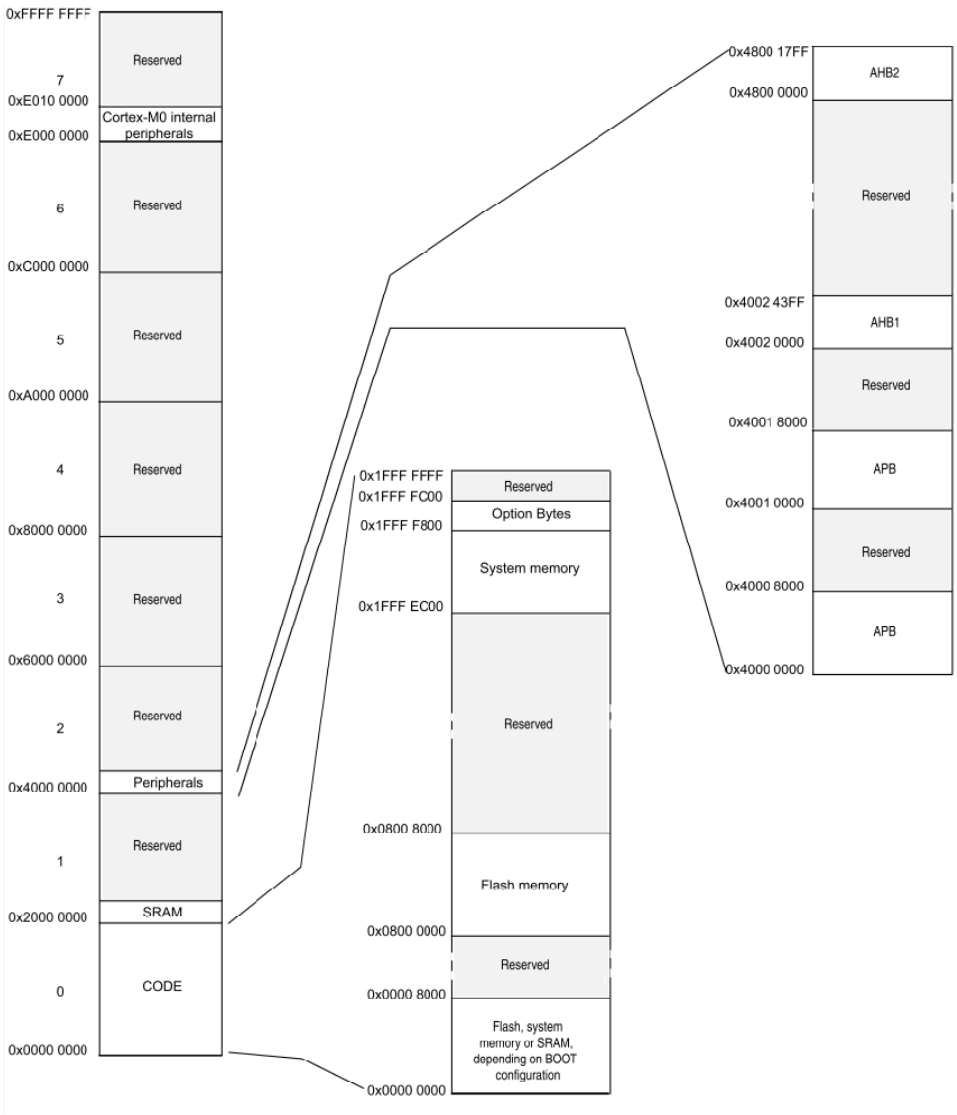
3.1 Structure diagram

ARMofCortex™-M0The processor is the latest generation of embedded32bitRISCprocessor, which is a low-cost, ultra-low-power MCUplatform while delivering superior computing performance and advanced system response to interrupts.HK32F030Series products have built-inCortex™-M0core, so it is compatible with allARMTools and software are compatible.

The functional block diagram of this series of products is as follows:



3.2 memory map



3.3 Built-in flash memory

Internally integrated up to64KByteFlash memory for storing programs and data.

3.4 CRCcomputing unit

Internally integrates an independentCRCThe hardware computing unit reduces the burden on user applications and provides the ability to accelerate processing.

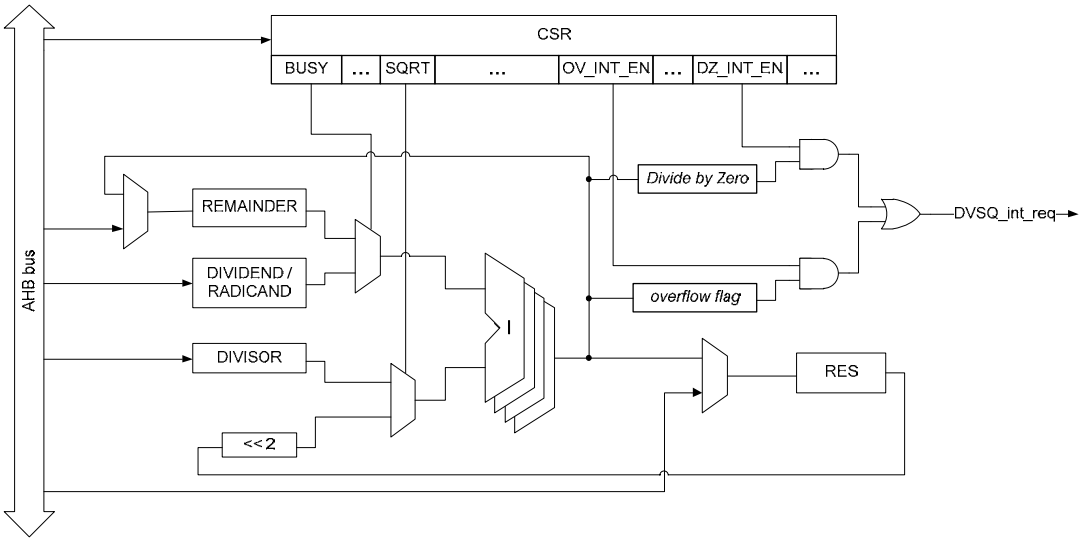
CRC(Cyclic Redundancy Check) computational unit uses a configurable polynomial from a32bits generated in the data word CRC code.

3.5 DIVSQRTcomputing unit

DVSQAccelerator support32/32unsigned division of (SDIV)and signed division (UDIV),and32Bit unsigned square root operation. Division operations are supported at the same timeMODOperation, after the operation is completed, the quotient and remainder are simultaneously updated to the corresponding registers for software to read.

- support32Bit signed and unsigned division, supports32Bit root operation. at the same moment,DVSQThe accelerator cannot support division and square root operations at the same time, and can only choose one of the two to execute.32/32Signed/unsigned integer division (gets both quotient and remainder). Unsigned square root operation, high precision square root operation can be selected by software.
- Pipeline design, done every clock2bitsoperation.
- The calculation time varies depending on the calculation data.
- Divide by zero interrupt and overflow interrupt are supported.

The structure is as follows:



3.5.1 Description of the division operation

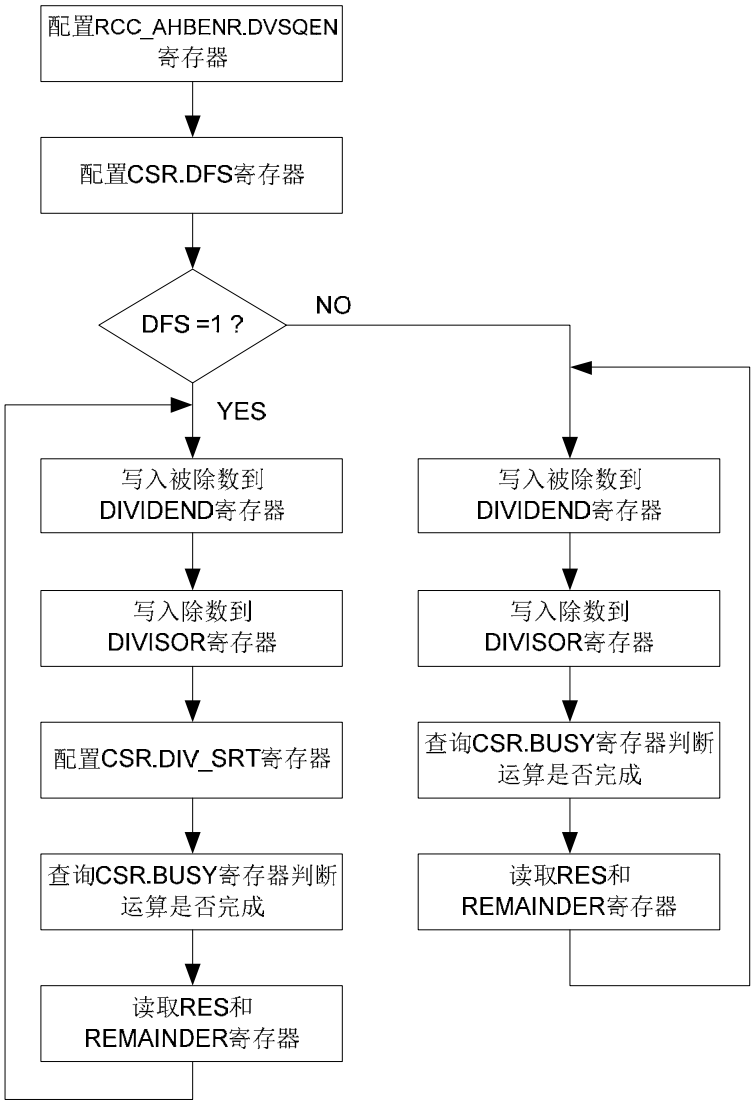
division operation

result registerRESand remainder registerREMAINDERThe value held in is always in two's complement format. If performing an unsigned division operation, thenRESregister andREMAINDERThe values in the registers are all positive numbers. If you perform signed division, thenRESregister andREMAINDERThe sign bit of the register is determined by the input operand:

- The quotient is negative if the sign bits of the dividend and the divisor are different; otherwise, the quotient is positive. The
- sign bit of the remainder is always the same as the sign bit of the divisor.

Operating procedures

The division operation can be started in two ways, fast start and non-fast start and non-fast start. The operation flow diagram of the division operation is as follows:



3.5.2 Division running time

DVSQThe accelerator determines the operation time according to the dividend data, so as to obtain the operation result as soon as possible. The specific operation time is as follows, in which the operation time is defined as the number of clock cycles from the start of the operation to the operation result, that is CSR.BUSY for the high duration.

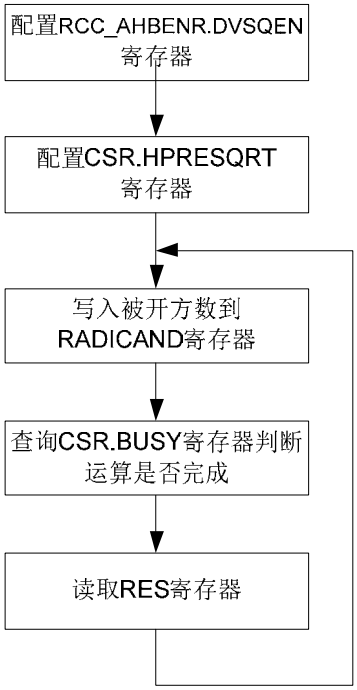
the absolute value of the dividend	Operation time [cycle number]
(01,1x)xx_xxxx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	17
00(01,1x)_xxxx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	16
0000_(01,1x)xx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	15
0000_00(01,1x)_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	14
0000_0000_(01,1x)xx_xxxx__xxxx_xxxx_xxxx_xxxx	13
0000_0000_00(01,1x)_xxxx__xxxx_xxxx_xxxx_xxxx	12
0000_0000_0000_(01,1x)xx__xxxx_xxxx_xxxx_xxxx	11

0000_0000_0000_00(01,1x)__xxxx_xxxx_xxxx_xxxx	10
0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx_xxxx	9
0000_0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx	8
0000_0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx	7
0000_0000_0000_0000_0000_00(01,1x)_xxxx_xxxx	6
0000_0000_0000_0000_0000_0000_(01,1x)xx_xxxx	5
0000_0000_0000_0000_0000_0000_00(01,1x)_xxxx	4
0000_0000_0000_0000_0000_0000_0000_(01,1x)xx	3
0000_0000_0000_0000_0000_0000_0000_00(01,1x)	2
0000_0000_0000_0000_0000_0000_0000_0000	1

3.5.3 Root operation description

DVSQThe accelerator can only perform unsigned square root, so when the square root operation is performedRADICANDandRES The values in are all unsigned numbers.

Operating procedures



square root run time

DVSQThe accelerator determines the operation time according to the squared number, and at the same timeCSR.HPRESQRTAlso affects the square root operation time. The specific time is as follows, where the operation time is defined as the number of clock cycles from the start of the operation to the result of the operation, that is,CSR.BUSYfor the high duration.

whenCSR.HPRESQRTfor0Time::

squared	Operation time [number of cycles]
(01,1x)xx_xxxx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	17

00(01,1x)_xxxx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	16
0000_(01,1x)xx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	15
0000_00(01,1x)_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	14
0000_0000_(01,1x)xx_xxxx__xxxx_xxxx_xxxx_xxxx	13
0000_0000_00(01,1x)_xxxx__xxxx_xxxx_xxxx_xxxx	12
0000_0000_0000_(01,1x)xx__xxxx_xxxx_xxxx_xxxx	11
0000_0000_0000_00(01,1x)__xxxx_xxxx_xxxx_xxxx	10
0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx_xxxx	9
0000_0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx	8
0000_0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx	7
0000_0000_0000_0000_0000_00(01,1x)_xxxx_xxxx	6
0000_0000_0000_0000_0000_0000_(01,1x)xx_xxxx	5
0000_0000_0000_0000_0000_0000_00(01,1x)_xxxx	4
0000_0000_0000_0000_0000_0000_0000_(01,1x)xx	3
0000_0000_0000_0000_0000_0000_0000_00(01,1x)	2
0000_0000_0000_0000_0000_0000_0000_0000	1

whenCSR.HPRESQRTfor1Time:

squared	Operation time [number of cycles]
(01,1x)xx_xxxx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	33
00(01,1x)_xxxx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	32
0000_(01,1x)xx_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	31
0000_00(01,1x)_xxxx_xxxx__xxxx_xxxx_xxxx_xxxx	30
0000_0000_(01,1x)xx_xxxx__xxxx_xxxx_xxxx_xxxx	29
0000_0000_00(01,1x)_xxxx__xxxx_xxxx_xxxx_xxxx	28
0000_0000_0000_(01,1x)xx__xxxx_xxxx_xxxx_xxxx	27
0000_0000_0000_00(01,1x)__xxxx_xxxx_xxxx_xxxx	26
0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx_xxxx	25
0000_0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx	twenty four
0000_0000_0000_0000_0000_(01,1x)xx_xxxx_xxxx	twenty three
0000_0000_0000_0000_0000_00(01,1x)_xxxx_xxxx	twenty two
0000_0000_0000_0000_0000_0000_(01,1x)xx_xxxx	twenty one
0000_0000_0000_0000_0000_0000_00(01,1x)_xxxx	20
0000_0000_0000_0000_0000_0000_0000_(01,1x)xx	19
0000_0000_0000_0000_0000_0000_0000_00(01,1x)	18
0000_0000_0000_0000_0000_0000_0000_0000	1

3.5.4 interrupt

DVSQThe two interrupt sources inside the accelerator share the same interrupt number in the chip. When the system detects an interrupt request, it needs to read the interrupt request.CSRRegister to determine whether it is a divide-by-zero interrupt or an overflow interrupt. At the same time, only one of the divide-by-zero interrupt and the overflow interrupt can occur.

Signed division overflow breaks:

- can be configured byCSR.OV_INT_ENenable or disable. When the dividend of signed number division is
- 0x8000_0000, the divisor is0xFFFF_FFFF, the interrupt request will be set by hardware.

- This interrupt condition can be cleared by software or hardware:
  - Software configurationCSR.DV_FLAGfor0.
  - Start the next division or square root operation.

remove0Interrupt:

- can be configured byCSR.OV_INT_ENenable or disable. When the
- divisor is0, the interrupt request will be set by hardware.
- This interrupt request can be cleared by software or hardware:
  - Software configurationCSR.DZ_FLAGfor0.
  - Start the next division or square root operation.

3.5.5 Precautions

Division operation:

- becauseDIVIDENDregister andDIVISORThe value of the register is not changed by hardware during the operation, so software needs to be careful when writing to these two registers by byte or halfword. such as software byte writeDIVIDEND[7:0] back, DIVIDENDhigh in the registertwenty fourBit is the value written in the last division operation, low8bit is the newly written value.
- When division is configured for fast start, whether it is a byte write, half word write, or word writeDIVISORregister will start the division operation.

Square root operation:

- Whether it is byte writing, half-word writing or word writingDIVISORregister will start the division operation.

The result reads:

- if inDVSQAccess when the operation has not been completedRESandREMAINDERThe register will make the bus in a waiting state, and it cannot be interrupted correspondingly in the waiting state. Software can pollCSR.BUSY state to judgeRESandREMAINDERwhether the value is ready.
- if inDVSQAccess when the operation has not been completedDIVIDEND/DIVISOR/RADICANDThe registers also hold the bus in a wait state.

3.6 SRAM

Internal integration up to10KByte SRAM,CPUFast read and write access with zero wait cycles meets the needs of most applications.

3.7 NVICs

Built-in nested vectored interrupt controller capable of handling up to32maskable interrupt channels (excluding16indivual Cortex™-M0the interrupt line) and4priority. The module provides flexible interrupt management capabilities with minimal interrupt latency.

● tightly coupledNVICInterrupt response processing with low latency

● Interrupt vector entry address directly into the kernel

● tightly coupledNVICinterface

● Enable early processing of interrupts

● Handle late-arriving higher-priority interrupts

● Support interrupt tail link function

● Automatically save processor state

● Automatic recovery when interrupt returns without additional instruction overhead

3.8 EXTI

Extended Interrupt/Event Controller containstwenty fourRoot is used to generate interrupt/event requests and wake up the system on the edge-detected interrupt line. Each interrupt line can be independently configured to select a trigger event (rising edge, falling edge, or edge) and can be individually masked. Pending registers are used to hold the status of interrupt requests.EXTIExternal interrupt lines with pulse width less than the internal clock period can be detected. The external interrupt line has a maximum of16root, available from up to39indivualGPIOselect Connect.

3.9 clock

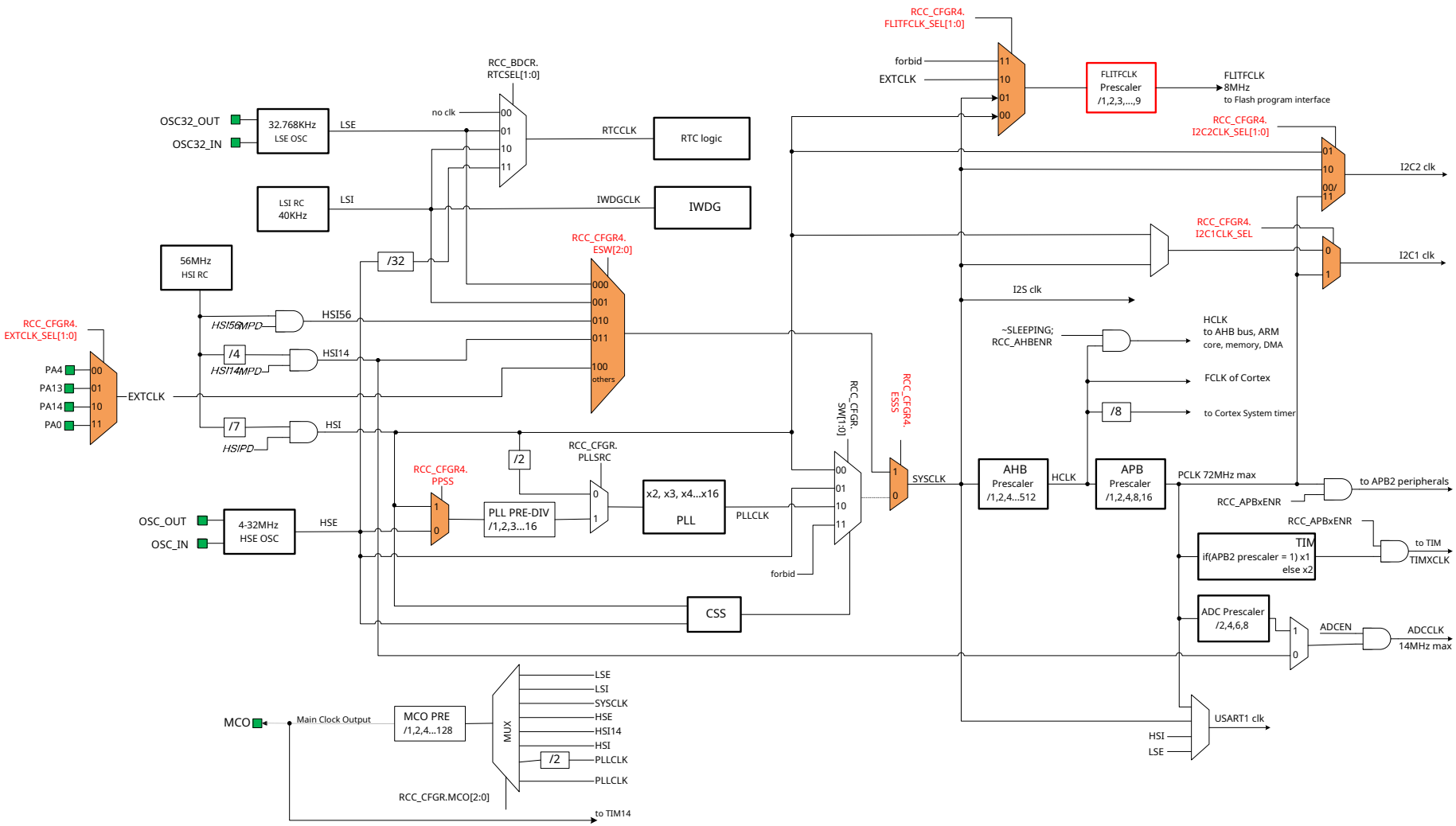
The selection of the system clock is made at startup, and the internal56MHzofRCOscillator divided to8MHz, is selected as the defaultCPUclock, and then other clock sources can be selected as the system clock. existCSSAfter the function is turned on, when the externalHSEWhen the clock fails, it will be isolated and the corresponding interrupt will be generated. Likewise, when needed,PLL Clock complete interrupt management (eg when an external oscillator fails). Has multiple prescalers for configurationAHBfrequency, high speedAPB(APB2)and low speedAPB(APB1)area.AHBandAPBThe highest frequency is 72MHz.

PLLPrescaled input clockHSEandHSIOptional.

forCPUMore clock sources are designed for the operating frequency of the device, and it also provides customers with light, flexible and diverse working modes.

- 32KHz LSEcan be used asCPUclock
- 40KHz LSIcan be used asCPUclock
- 4roadGPIOpin (PA0/PA4/PA13/PA14) input can be used asCPUclock

The clock structure is as follows:


RCC_CFGR4.
FLITFCLK_SEL[1:0]
forbid
EXTCLK
11
10
01
00
FLITFCLK
Prescaler
/1,2,3,...,9
FLITFCLK
8MHz
to Flash program interface
RCC_BDCR.
RTCSEL[1:0]
OSC32_OUT
OSC32_IN
32.768KHz
LSE OSC
LSE
no clk
00
01
10
11
RTCCLK
RTC logic
LSI RC
40KHz
LSI
IWDGCLK
IWDG
RCC_CFGR4.
I2C2CLK_SEL[1:0]
01
10
00/
11
I2C2 clk
RCC_CFGR4.
I2C1CLK_SEL
0
1
I2C1 clk
56MHz
HSI RC
/32
RCC_CFGR4.
ESW[2:0]
000
001
010
011
100
others
I2S clk
HSI56MPD
HSI56
RCC_CFGR4.
EXTCLK_SEL[1:0]
PA4
PA13
PA14
PA0
00
01
10
11
EXTCLK
/4
HSI14MPD
HSI14
~SLEEPING;
RCC_AHBENR
HCLK
to AHB bus, ARM
core, memory, DMA
FCLK of Cortex
/8
to Cortex System timer
/7
HSIPD
HSI
/2
RCC_CFGR.
PLLSRC
RCC_CFGR4.
PPSS
RCC_CFGR.
SW[1:0]
RCC_CFGR4.
ESSS
SYSCLK
AHB
Prescaler
/1,2,4...512
HCLK
APB
Prescaler
/1,2,4,8,16
PCLK 72MHz max
to APB2 peripherals
RCC_APBxENR
OSC_OUT
OSC_IN
4-32MHz
HSE OSC
HSE
PLL PRE-DIV
/1,2,3...16
x2, x3, x4...x16
PLL
PLLCLK
forbid
RCC_APBxENR
TIM
if(APB2 prescaler = 1) x1
else x2
to TIM
TIMXCLK
CSS
ADC Prescaler
/2,4,6,8
ADCEN
ADCCLK
14MHz max
MCO
Main Clock Output
MCO PRE
/1,2,4...128
MUX
LSE
LSI
SYSCLK
HSE
HSI14
HSI
/2
PLLCLK
PLLCLK
USART1 clk
HSI
LSE
RCC_CFGR.MCO[2:0]
to TIM14

3.10 Bootmodel

At startup, the bootstrap pins are used to select one of three bootstrap modes

● Boot from user flash

● Bootstrapping from system memory

● from the insideSRAMbootstrapping

The bootloader is stored in system memory and can be accessed viaUSART1/USART2Reprogram the flash.

3.11Power supply scheme

- VDD = 2.0~5.5V:VDDpin isI/Opins and internalLDOpowered by VDDA = 2.0~
- 5.5V:forADC, The temperature sensor analog part provides power

3.12power monitor

Internally integrated power-on reset (POR)/Power-down reset (PDR)circuit, which is always in working condition to ensure that the system is powered over2Vtime work. whenVDDlower thanPOR/PDRWhen the threshold is set, the device is placed in the reset state without using an external reset circuit. The device also has a programmable voltage monitor (PVD), which monitorsVDDpowered and with the threshold VPVD compare whenVDDbelow or above the thresholdVPVDWhen an interrupt occurs, the interrupt handler can issue a warning message or put the microcontroller into safe mode.PVDThe function needs to be enabled through the program enable.

3.13low power mode

The chip supports multiple power consumption modes

● Sleep Mode: sleep mode

in sleep mode,onlyCPUStop, all peripherals are active and can wake up on interrupt/eventCPU.

● Stop Mode: stop mode

in keepingSRAMand the register contents are not lost, the shutdown mode can achieve the lowest power consumption. In shutdown mode, all internal clocks are turned off,PLL,HSIandHSEofRCThe oscillator is turned off. can be configured by eitherEXTIsignal wakes the microcontroller from shutdown mode,EXTIsignal can be16externalI/O one of the mouths,PVD Output,RTCAlarm clock,UARTheader matching andI2CAddress matches.

● Standby Mode: Standby mode

The lowest power consumption can be achieved in standby mode. internalLDOis closed, so all internal1.5VPart of the power supply is cut off;PLL,HSIandHSEofRCThe oscillator is also turned off; after entering standby mode,SRAMThe contents of the and register will disappear, but the contents of the backup register will remain, and the standby circuit will still work. The conditions for exiting from standby mode are:NRSTexternal reset signal on theIWDGreset,WKUPedge on the pin orRTC's alarm clock is up.

Wakeuppins have6pins are optional. they are, respectivelyPC13/PA0/PA6/PA7/PA9/PA10.

3.14 DMA

flexible5road generalDMAMemory-to-memory, device-to-memory, and memory-to-device data transfers can be managed.1indivualDMAThe controller supports the management of the ring buffer, avoiding the interruption when the controller transfer reaches the end of the buffer.

Dedicated hardware for each channelDMARequest logic, and each channel can be triggered by software at the same time; transmission length, Both the source and destination addresses of the transfer can be individually set by software.DMAAvailable for major peripherals:SPI,I2C,USART, timerTIMx,SDIOandADC.

3.15 RTCclock

HK32F030series chipLQFP64,LQFP48,LQFP32,TSSOP20Packages are not independentVBAT pins, as long asVDDhave electricity,VBATdomain will still work fine, providingStandByLow power function.

RTCis an independentBCDTimer/Counter. Its main features are as follows:

- Calendar has subseconds, seconds, minutes, hours (12ortwenty fourFormat) , day of week, day, month, year in the formatBCD (binary decimal number).
- Auto Adjust Monthly Yes28,29(leap year),30still31sky. The programmable
- alarm clock has the ability to wake up from stop and standby modes.
- Runtime correction1arrive32767indivualRTCclock pulse. This can be used toRTCSynchronized with the master clock.
- The digital calibration circuit has1 ppmresolution to compensate for quartz crystal inaccuracies.
- Two tamper detection pins have programmable filters. When a tampering event is detected,MCU stop and can be stopped wake up from standby mode.
- The timestamp feature can be used to save calendar content. This function can be triggered by an event on the timestamp pin, or by a tampering event. When a timestamp event is detected,MCU Wake-up from stop and standby modes.
- Reference Clock Detection: A more accurate second clock source can be used (50or60Hz) to improve the accuracy of the calendar

3.16independent watchdog

The independent watchdog is based on a12bit down counter and a8bit prescaler, which consists of an internal independent40kHzofRC oscillator provides the clock because thisRCThe oscillator is independent of the main clock, so it can operate in shutdown and standby modes. It can be used as a watchdog to reset the entire system in the event of a problem, or as a free timer to provide time-out management for applications. The watchdog can be configured to be a software or hardware enabled watchdog by selecting the byte. In debug mode, the counters can be frozen.

3.17window watchdog

There is a window watchdog inside7bit down counter and can be set to free-running. It can be used as a watchdog to reset the entire system in the event of a problem. It is driven by the master clock and has an early warning interrupt function. In debug mode, the counter can be frozen.

3.18 System Ticktimer

This timer is dedicated to the operating system and can also be used as a standard down counter. It has the following properties.

- twenty fourbit down counter
- Reload function
- When the counter is0can generate a maskable interrupt when
- Programmable clock source

3.19timer

HK32F030x4/x6/x8The device includes up to five general purpose timers and one advanced control timer.

timer Types of	**Timer**	counter Resolution	counter Types of	prescaler coefficient	**DMA** request generation	capture/Compare aisle	Complementary output
advanced control	TIM1	16bit	increase, decrease, increment/decrement	1and65536 any between integer	have	4	have
Universal	TIM3	16bit	increase, decrease, increment/decrement	1and65536 any between integer	have	4	without
	TIM14	16bit	increment	1and65536 any between integer	without	1	without
	TIM15	16bit	increment	1and65536 any between integer	have	2	without
	TIM16	16bit	increment	1and65536 any between integer	have	1	have
	TIM17	16bit	increment	1and65536 any between integer	have	1	have
basic	TIM6	16bit	increment	1and65536 any between integer	have	0	without

3.19.1basic timer

TIM6

TIM6is used to generateDACTrigger signal, can also be used as a general16Bit time base counter.

3.19.2General purpose timer

Every general purpose timer can be used to generatePWMoutput, or as a simple time base.

TIM3

TIM3based on a16Bit auto-reload up/down counters and a16bit prescaler. they all have4independent channels for input capture/output compare,PWM, Single-pulse mode output. In the largest package, up to12 input capture/output compare/PWM.

TIM3The general purpose timer can be linked with the timer link functionTIM1Advanced control timers work together to provide synchronization or event chaining capabilities.TIM3can generate independentDMAask. These timers are capable of handling quadrature (incremental) encoder signals as well as1arrive3digital output of a Hall-effect sensor. In debug mode, its counters can be frozen.

TIM14,TIM15

The timer is based on a16bit auto-reload incrementing counter and a16bit prescaler.TIM14has a single channel for input capture/output compare,PWMor single-pulse mode output. In debug mode, its counters can be frozen.TIM14can produceDMAask,TIM15not.

TIM16andTIM17

Two timers based on one16bit auto-reload incrementing counter and a16bit prescaler. They each have a single channel for input capture/output compare,PWMor single-pulse mode output.TIM16andTIM17Complementary outputs with dead time generation and independentDMARequest generation function. In debug mode, its counters can be frozen.

3.19.3Advanced Timer

Advanced Control Timer (TIM1)can be seen as assigned to6three-phase channelPWMThe generator can also be used as a complete general-purpose timer. Four independent channels can be used for:

- Input capture
- output comparison
- producePWM(edge or center alignment mode)
- Single pulse output
- ComplementaryPWMOutput, with programmable dead-band insertion function

configured as16bit standard timer, it is associated withTIMxA timer has the same function. configured as16bitPWMgenerator, it has full modulation capability (0~100%). In debug mode, the counter can be frozen. Many functions are the same as the standardTIMThe timer is the same, and the internal structure is also the same, so the advanced control timer can be connected with the timer link functionTIMTimers work together to provide synchronization or event chaining capabilities.

3.20 IICbus

2indivualI2Cbus interface, capable of working in multi-master and slave mode, supporting standard mode (up to100 kbit/s) ,fast mode (maximum400 kbit/s) and Speed mode (maximum1 Mbit/s)have20mAoutput driver.

I2CInterface support7bit or10bit addressing,7Dual-slave addressing is supported in bit-slave mode.

I2CprovidedSMBUS 2.0andPMBUS 1.1Hardware support for:ARPCapability, Host Notification Protocol, Hardware CRC(PEC) generate/validate, timeout validation,ALERTProtocol management.

I2CThere is also an independentCPUclock domain clock, such thatI2CWake-up from stop mode on address match MCU.

Programmable analog and digital noise filters.

	analog filter	digital filter
Suppressed pulse width	≥ 50ns	from1arrive15indivualI2CProgrammable length of peripheral clock
advantage	Still available in stop mode	1.Additional filtering capabilityvsstandard requirements. 2.stable length
shortcoming	Variation with temperature, voltage, process change	

3.21 USART

The device has built-in2A universal synchronous/asynchronous transceiver (USART1), with a communication rate of up to6 Mbit/s. it providesCTS,RTS,RS485 DEHardware management of signaling, multiprocessor communication modes, master synchronous communication, and single-wire half-duplex communication modes.USART1Also supports smart card communication (ISO 7816),IrDA SIR ENDEC,LINmaster/slave capability, auto-baud feature, withCPUClock-independent clock domain, wake-up from stop modeMCU. USARTinterface can be usedDMAcontroller.

USARTcharacteristic	**USART1**
Modem hardware flow control	support
useDMAfor continuous communication	support
multiprocessor communication	support
Sync mode	support
SmartCardmodel	support
Single-wire half-duplex communication	support
IrDA SIR ENDECmodule	support
LINmodel	support
Dual clock domains and wake-up from stop mode	support
Receiver Timeout Interrupt	support
Modbuscommunication	support
Automatic baud rate detection	support
driver enabled	support

3.22 SPI

HK32F030have2indivualSPIinterface, up to18 Mbit/sCommunication can be slave and master mode, full duplex and half duplex communication mode.3A bit prescaler can generate8main mode frequencies, the frame can be configured as4bit to16bit.

standardI2Sinterface (withSPIMultiplexing) supports four different audio standards and can work in master or slave half-duplex communication mode. It can be configured as16,twenty four,32bit transfer, yes16bit or32Bit data resolution, synchronized by dedicated signal. by 8Bit programmable linear prescaler settings8kHzto192kHzaudio sampling frequency. When working in master mode, it can output sampling frequency for external audio components256times the clock.

SPIcharacteristic	SPI
hardwareCRCcalculate	support
Rx/Tx FIFO	support
NSSpulse mode	support
I2Smodel	support
TImodel	support

3.23 GPIO

eachGPIOPins can be configured by software as outputs (push-pull or open-circuit), inputs (with or without pull-up or pull-down), or other peripheral function ports. mostGPIOPins are shared with digital or analog peripherals. allGPIOThe pins have the ability to pass large currents. In case of need,I/OThe peripheral functions of the pins can be locked by a specific operation to avoid accidental writesI/Oregister.

3.24 ADCs

inline1indivual12bit analog/digital converter (ADC), eachADCshare up to16external channels for single-shot or scan conversion. In sweep mode, conversion on a selected set of analog inputs occurs automatically.

ADCAdditional logical functions on the interface include:

- Simultaneous sample and hold
- Cross sample and hold
- Single sampling

ADCcan useDMAoperate. The analog watchdog function allows very precise monitoring of one, multiple or all selected channels, and will generate an interrupt when the monitored signal exceeds a preset threshold. by the standard timer (TIMx)and Advanced Control Timer (TIM1) generated events, which can be cascaded internally to theADCstart trigger and injection trigger, the application can enableADConversions are synchronized with the clock.

3.25Temperature Sensor

The temperature sensor produces a voltage that varies linearly with temperature. The temperature sensor is internally connected to ADC1_IN16 is used to convert the sensor output to a digital value on the input channel.

3.26Internal reference voltage

Internal reference voltage (VREFINT)forADCand comparator provides a regulated voltage output.VREFINT Internally connected toADC_IN17input channel. The access mode is read-only.

3.27debug interface

inlineARMofSWJ-DPinterface that can implement serial lineSWDIO/SWCLKDebug interface.

4 Performance

4.1 Absolute Maximum Ratings

Maximum ratings are only short-term pressure values. And it is not advisable for the chip to operate at this value or any other condition beyond this recommended value. Exceeding the following maximum ratings may cause permanent damage to the chip. Exposure to maximum ratings for extended periods of time may affect chip reliability.

4.1.1 Limiting Voltage Characteristics

symbol	describe	minimum	maximum value	unit
V_{DD}-V_{SS}	External mains supply voltage (includesV_{DDA}andV_{DD})	- 0.5	6.0	V
V_{IN}	input voltage on pin	VSS-0.3	VDD+4.0	
|ΔVDDx|	Voltage difference between different supply pins	-	50	mV
$\|V_{SSX}-V_{SS}\|$	Voltage difference between different ground pins	-	50	

4.1.2 Limiting current characteristics

symbol	describe	maximum value	unit
I_{VDD}	go throughV_{DD}/V_{DDA}Total current of the power cord (supply current)[1]	150	mA
I_{VSS}	go throughVSSTotal current in ground wire (current flowing out)[1]	150	
I_{IO}	anyI/Oand the output sink current on the control pin	25	
	anyI/Oand the output source current on the control pin	- 25	
$I_{INJ(PIN)}$[2]	Injection current on pin[3]	±5	
$\Sigma I_{INJ(PIN)}$	allI/Oand the total injected current on the CONTROL pin[4]	±25	

Note1: All power (V_{DD},V_{DDA}) and ground (V_{SS},V_{SSA}) pins must always be connected to an external power supply within the allowable range.

Note2: Back-injected current can interfere with the analog performance of the device.

Note3:whenV_{IN}>V_{DD}, there is a forward injection current; whenV_{IN}< V_{SS}When there is a reverse injection current, the injection current must not exceed the specified range.

Note4: when severalI/OWhen there is injected current at the same time, $\sum I_{INJ(PIN)}$The maximum value of is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current.

4.1.3 Extreme temperature characteristics

symbol	describe	parameter value	unit
T_{STG}	Storage temperature range	– 45 to +150	°C
T_J	Maximum Junction Temperature	125	

4.2 Working parameters

4.2.1 Recommended working conditions

symbol	describe	minimum	maximum value	unit
f_{HCLK}	internalAHBClock frequency	0	72	MHz
f_{PCLK1}	internalAPB1Clock frequency	0	72	
f_{PCLK2}	internalAPB2Clock frequency	0	72	
V_{DD}	Standard working voltage	2	5.5	V
V_{DDA} [1]	Analog working voltage	2	5.5	V
T	Operating temperature	- 40	105	°C

4.2.2 Reset and Low Voltage Detection

Table 4-1Power-on Reset Characteristics

symbol	parameter	condition	minimum	Typical value	maximum value	unit
T_{delay}	rstnBuild time	-	-	40		us
$V_{Threshold}$	reset threshold	-	-	1.75		V

Table 4-2 PVDcharacteristic

symbol	parameter	condition	minimum	Typical value	maximum value	unit
V_{PVD}	Programmable Voltage Detector's Detection level selection (rising along)	PLS[2:0]=000	2.183	2.188	2.196	V
		PLS[2:0]=001	2.286	2.289	2.298	
		PLS[2:0]=010	2.393	2.399	2.407	
		PLS[2:0]=011	2.502	2.508	2.518	
		PLS[2:0]=100	2.621	2.629	2.639	
		PLS[2:0]=101	2.726	2.733	2.745	
		PLS[2:0]=110	2.839	2.846	2.855	
		PLS[2:0]=111	2.958	2.969	2.979	
	Programmable Voltage Detector's Detection level selection (falling along)	PLS[2:0]=000	2.116	2.119	2.125	
		PLS[2:0]=001	2.208	2.211	2.220	
		PLS[2:0]=010	2.305	2.310	2.320	
		PLS[2:0]=011	2.399	2.406	2.416	
		PLS[2:0]=100	2.506	2.512	2.521	
		PLS[2:0]=101	2.596	2.602	2.613	
		PLS[2:0]=110	2.693	2.701	2.710	
		PLS[2:0]=111	2.798	2.805	2.817	

4.2.3 Operating current characteristics

Table 4-3Operating current characteristics

model	condition	VDD@25°C			Unit
		2.0V	3.3V	5.0V	

Run mode	HCLK=96MHz, FLASH read3wait period,APB clockenable	21.505	22.63	22.85	mA
	HCLK=96MHz, FLASH read3wait period,APB clockdisable	12.908	13.232	13.301	mA
	HCLK=HSE 8MHz, FLASHread0wait week Expect,APBclockenable	3.151	3.418	3.533	mA
	HCLK=HSE 8MHz, FLASHread0wait week Expect,APBclockdisable	2.316	2.559	2.653	mA
	HCLK=LSI 40KHz	196	208	212	uA
	HCLK=LSE 32.768KHz	190	205	215	uA
Sleep mode	HCLK=96MHz APBclockdisable	5.199	5.441	5.483	mA
	HCLK=HSI 8MHz APBclockdisable	0.778	0.845	0.937	mA
Stop mode	LDOWorking at full speed HSE/HSI/LSEclosure	126	128	130	uA
	LDOlow power state HSE/HSI/LSEclosure	9.22	10.26	12.47	uA
Standby mode	LSI and IDWG on	1.13	1.64	3.17	uA
RTC Power consumption	RTC with LSE=32.768K	'-	1.0	'-	uA

4.2.4 External Clock Features

Table 4-4External high-speed clock features

symbol	parameter	condition	minimum	Typical value	maximum value	unit
f_{HSE_ext}	Clock frequency	-	1	8	25	MHz
V_{HSEH}	input pin high		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	input pin low		V_{SS}	-	0.3V_{DD}	
$Tw_{(HSE)}$	Active high/low time		5	-	-	ns
$Tr_{(HSE)}$ $Tf_{(HSE)}$	Rise/Fall Time		-	-	20	
$Cin_{(HSE)}$	Input capacitive reactance	-	-	5	-	pF
$DuCy_{(HSE)}$	duty cycle	-	45	-	55	%

Table 4-5External low-speed clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{LSE_ext}	Clock frequency	-	-	32.768	1000	kHz
V_{LSEH}	input pin high		0.7V_{DD}	-	V_{DD}	V
V_{LSEL}	input pin low		V_{SS}	-	0.3V_{DD}	

$T_{W(LSE)}$	Active high/low time		450	-	-	Ns
$T_{r(LSE)}$ $T_{f(LSE)}$	Rise/Fall Time		-	-	50	
$C_{in(LSE)}$	Input capacitive reactance	-	-	5	-	pF
$DuCy_{(LSE)}$	duty cycle	-	30	-	70	%

4.2.5 Internal Clock Characteristics

Table 4-6Internal fast clock feature

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Clock frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	duty cycle	-		45	-	55	%
ACC_{HSI}	Oscillator Accuracy	RCC_CRAfter register calibration		-	-	1	%
		Factory calibrated	T_A= –40 to 105 °C	- 2	-	2.5	%
			T_A= –40 to 85 °C	- 1.5	-	2.2	%
			TA = 0 to 70 °C	- 1.3	-	2	%
			TA = 25 °C	- 1.1	-	1.8	%
$T_{su(HSI)}$	Oscillator start-up time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	us
$I_{DD(HSI)}$	Oscillator power consumption			-	80	100	uA

Table 4-7Internal slow clock feature

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Clock frequency	30	40	60-	kHz
$t_{su(LSI)}$	Oscillator start-up time	-	-	85	us
$I_{DD(LSI)}$	Oscillator power consumption		0.65	1.2	uA

4.2.6 PLLcharacteristic

Table 4-8 PLLscharacteristic

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	input clock frequency	1	8.0	25	MHz
	Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	output clock frequency	16	-	72	MHz
t_{LOCK}	Phase lock time	-	-	200	us
Jitter	Cyclic jitter	-	-	300	ps

4.2.7 Memory characteristics

Table 4-9Memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	Half word write time		25		μs
	word writing time		33		μs
T_{ERASE}	Half Page Erase Time		9.2		ms
	Page Erase Time		4.6		
	Chip Erase Time		38		ms
IDD_{PROG}	Nibble Write Current	-	-	5	mA
IDD_{ERASE}	Page/Chip Erase Current	-	-	2	mA
IDD_{READ}	read current @24MHz	-	2	3	mA
	read current @1MHz	-	0.25	0.4	mA
V_{IL}	input low voltage	-		$0.1V_{DD}$	
V_{IH}	input high voltage	$0.9V_{DD}$			
V_{OL}	output low voltage			$0.1V_{DD}$	
V_{OH}	output high voltage	$0.9V_{DD}$			
N_{END}	erasing life	1			thousand times
t_{RET}	data retention time	20			year

1. Typical values refer to1.5V, TTProcess and temperature25°CUnder conditions.

4.2.8 IOPin Characteristics

Table 4-10 IOPin DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	input high level	V_{DD}>2V	0.42*(V_{DD} - 2V) + 1V		5.5	V
		V_{DD}≤2V			5.2	
V_{IL}	input low level		- 0.3		0.32*(V_{DD}-2V)+0.75V	V
V_{hys}	Schmitt trigger voltage Hysteresis		5%V_{DD}	-	-	mV
I_{lkg}	Input leakage current	V_{IN}=5V	-	-	3	uA
R_{PU}	weak pull-up equivalent resistor	V_{IN}=V_{SS}	30	40	50	KΩ
R_{PD}	weak pull-down equivalent resistor	V_{IN}=V_{DD}	30	40	50	KΩ
C_{IO}	I/O pin capacitance		-	5	-	pF

Table 4-2 IOPin AC Characteristics

Mode	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DD}=2V to 5.5V	-	2	MHz
	$t_{f(IO)out}$	output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DD}=2V to 5.5V	-	10	MHz

	$t_{f(IO)out}$	output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Maximum frequency	C_L=30pF, V_{DD}=2.7V to 5.5V	-	50	MHz
			C_L=50pF, V_{DD}=2.7V to 5.5V		30	
			C_L=50pF, V_{DD}=2V to 2.7V		20	
	$t_{f(IO)out}$	output high to low level fall time	C_L=30pF, V_{DD}=2.7V to 5.5V	-	5	ns
			C_L=50pF, V_{DD}=2 .7V to 5.5V		8	
			C_L=50pF, V_{DD}=2V to 2.7V		12	
	$t_{r(IO)out}$	output high to low level rise time	C_L=30pF, V_{DD}=2.7V to 5.5V	-	5	ns
			C_L=50pF , V_{DD}=2.7V to 5.5V		8	
			C_L=50pF, V_{DD}=2V to 2.7V		12	

4.2.9 TIMCounter Features

Table 4-3 TIMscount**device characteristics**

Symbol	Conditions	Min	Max	Unit
Tres(TIM)	Timer resolution time	1	-	$T_{TIMxCLK}$
FEXT	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}$/2	MHz
RESTIM	Timer resolution	-	16	bit
Tcounter	16-bit counter clock period when internal clock is selected	1	65536	$T_{TIMxCLK}$
TMAX_COUNT	Maximum possible count	-	65536x65536	$T_{TIMxCLK}$

1. $f_{TIMxCLK}$= 72MHz

4.2.10 ADCscharacteristic

Table 4-4 ADCscharacteristic

Parameter	Conditions	Min	Typ	Max	Unit
Full scale range	SDIF=0	vrefn	-	vrefp	V
	SDIF=1	2*(vrefp-vrefn)			V
Input signal common mode		(vrefp-vrefn)/2			V
Input sample capacitance	-	-	5	-	pF
Input switch equivalent impendence(Rs)	-	-	-	1000	Ohm
Positive reference voltage (vrefp)	-	AVDD	AVDD	AVDD	V
Negative reference voltage (vrefn)	-	0	0	0.1	V
Analog Supply voltage	-	2.0	3.3	5.5	V
Digital Supply voltage	-	1.35	1.5	1.65	V
Current Consumption AVDD	SDIF=1,@ 1Msps	-	110	-	uA
Current Consumption VDD		-	40	-	uA

Current Consumption vrefp		-	35	-	uA
Clock period(t_{clkp})		3333	71.4	23.8	Ns
The high level time of clock(t_{clkh})	-	40%	50%	60%	T_{clkp}
The time delay from rising edge of clock to rising edge of EOC(t_{eocr})	-	0.8	-	3	ns
The time delay from rising edge of clock to falling edge of EOC (t_{eocf})	-	0.8	-	3	ns
The time delay from rising edge of EOC to the data is valid at data bus B(t_{data})	-	1.2	-	4	ns
The setup time of SOC(t_{socs})	-	-	0.7	-	ns
The hold time of SOC(t_{soch})	-	-	0.7	-	ns
The time of Sampling and converting (t_{sp+con})	-	-	14	-	t_{clkp}
The time of sample(ts)	-	-	1.5	-	t_{clkp}
THD	-	-	- 72	-	db
SNDR	-	-	68	-	db
DNL	-	- 1	-	+ 1	LSB
INL	-	- 1.5	-	+ 1.5	LSB
offset error	-	- 16	-	16	LSB

4.2.11Temperature sensor characteristics

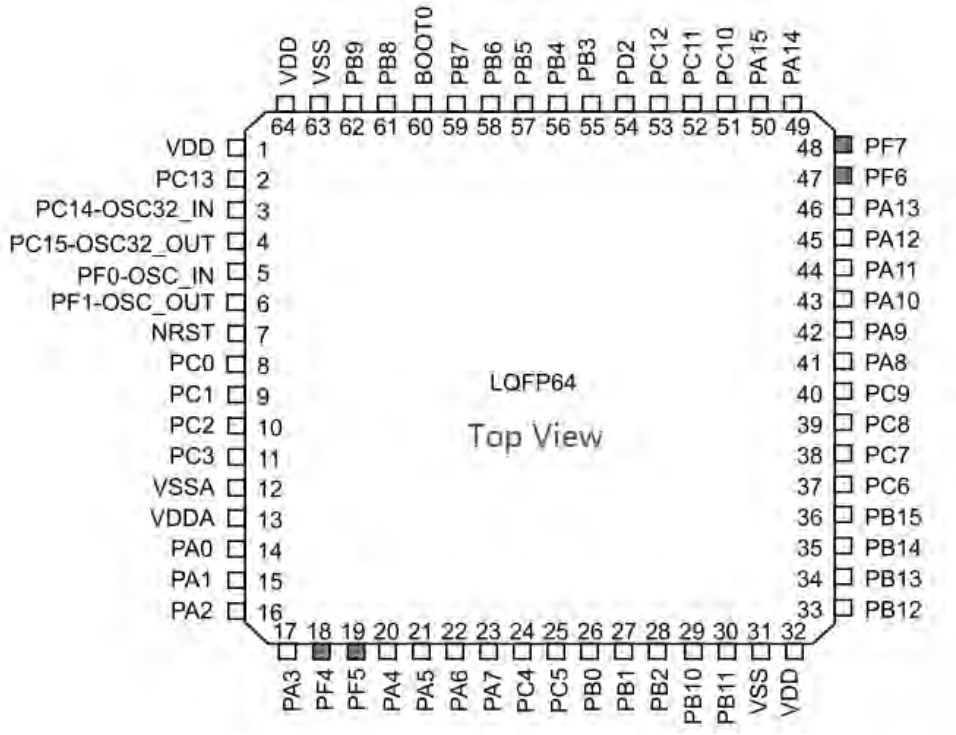
Table 4-5Temperature sensor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Analog Supply voltage	-	2.2	3.3	5	V
Digital Supply voltage	-	1.35	1.5	1.65	
Current Consumption	AVDD	-	150	-	uA
Power down leakage current	en='0'	-	-	1	
Power switch control voltage (Ven)	Power down	-	0	-	V
	Power on	-	1	-	Vddl
Sensor linearity with temperature	-	-	±1	±2	°C
Sensor output voltage	at 25°C	1.34	1.43	1.52	V
Sensor Gain	-	4.0	4.3	4.6	mV/°C
Output load capacitor	-	-	-	20	Pf
Output current	-	- 40	-	+ 40	uA
Power up time(t_{START})	-	4	-	10	us

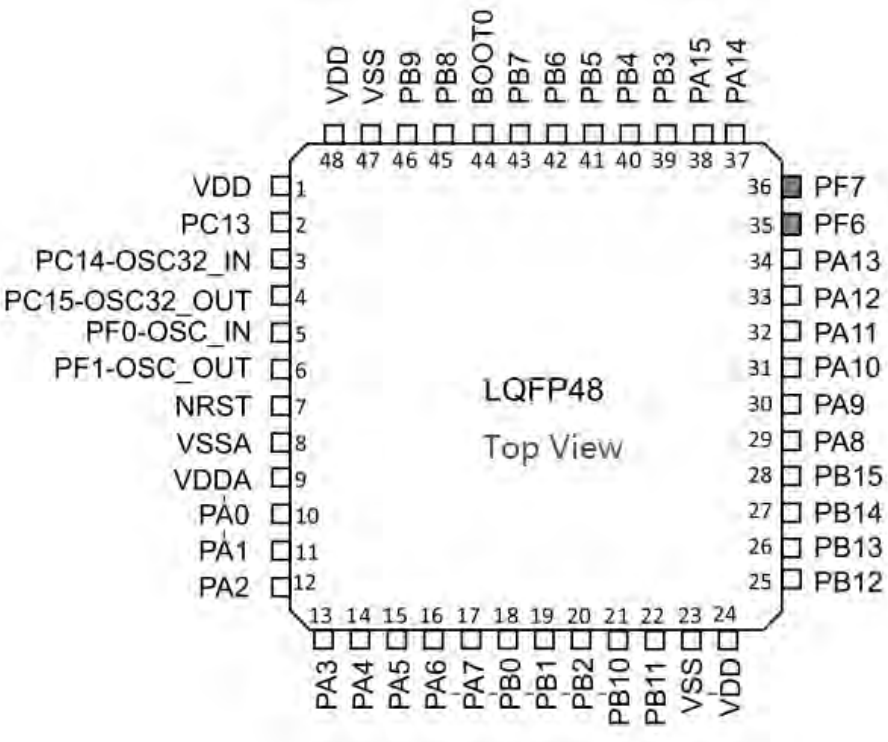
5 Pin Definition

HK32F030DefinedLQFP64/LQFP48/LQFP32/TSSOP20Four packages, the pin definitions are as follows.

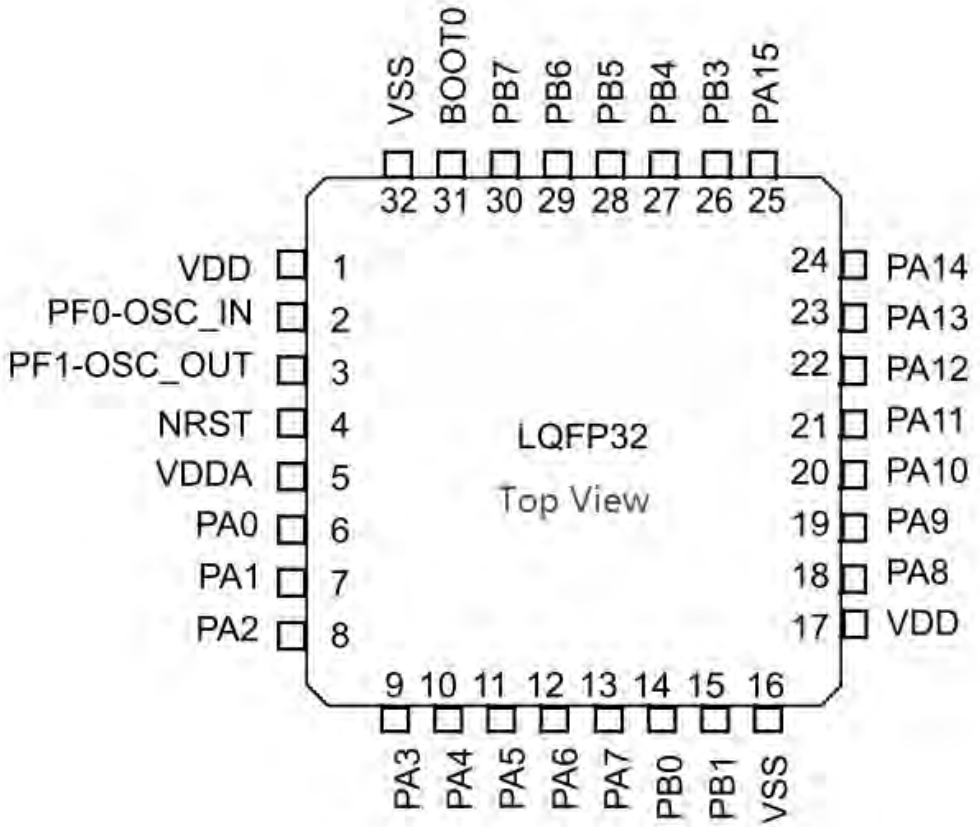
LQFP64packagePin-out



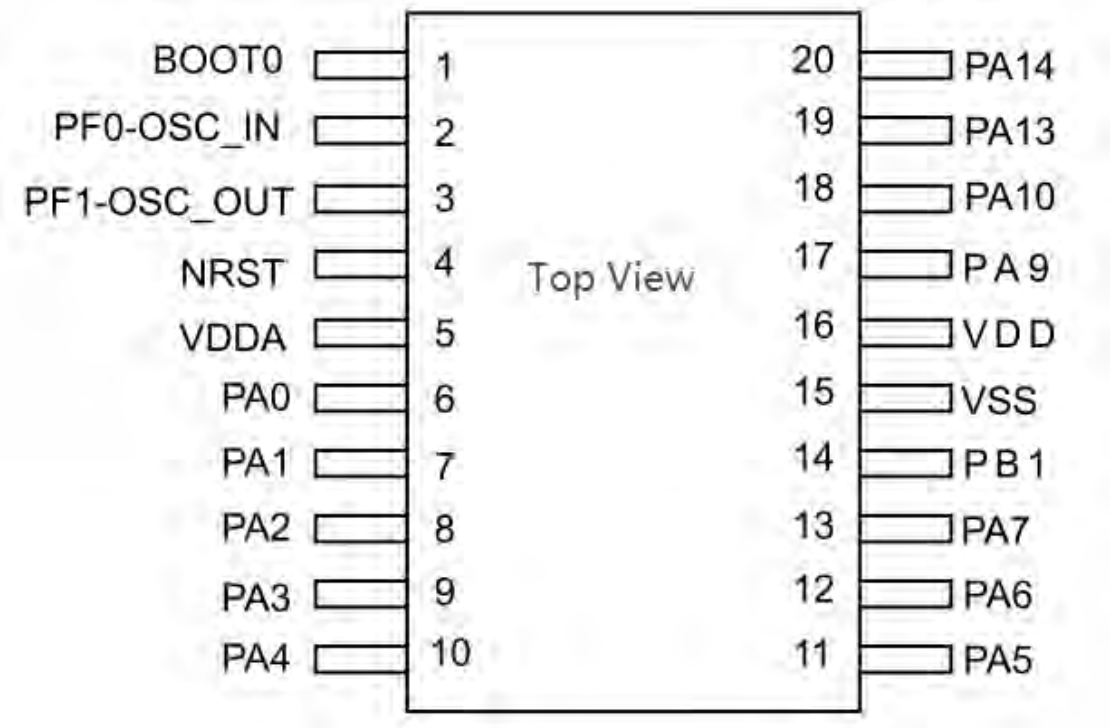
LQFP48packagePin-out



LQFP32packagePin-out



TSSOP20packagePin-out



The pin definitions are as follows

Pin number				Pin Name (Function after reset)	Pin type	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20			Alternate functions	Additional functions
1	1	-	-	VDD	S	Power Supply	
2	2	-	-	PC13	I/O	-	RTC_TAMP1 RTC_TS RTC_OUT WKUP2
3	3	-	-	PC14	I/O	-	OSC32_IN
4	4	-	-	PC15	I/O	-	OSC32_OUT
5	5	2	2	PF0	I/O	I2C1_SDA	OSC_IN
6	6	3	3	PF1	I/O	I2C1_SCL	OSC_OUT
7	7	4	4	NRST	I/O	Reset input/internal reset output, active low	
8	-	-	-	PC0	I/O	EVENTOUT	ADC_IN10
9	-	-	-	PC1	I/O	EVENTOUT	ADC_IN11
10	-	-	-	PC2	I/O	EVENTOUT SPI2_MISO	ADC_IN12
11	-	-	-	PC3	I/O	EVENTOUT SPI2_MOSI	ADC_IN13
12	8	-	-	VSSA	S	Analogy ground	
13	9	5	5	VDDA	S	Analogy Power Supply	
14	10	6	6	PA0	I/O	USART1_CTS	ADC_IN0 RTC_TAMP2 WKUP1 CKI_4
15	11	7	7	PA1	I/O	USART1_RTS USART2_RTS EVENTOUT TIM15_CH1N	ADC_IN1
16	12	8	8	PA2	I/O	USART1_TX USART2_TX TIM15_CH1	ADC_IN2 WKUP4
17	13	9	9	PA3	I/O	USART1_RX USART2_RX TIM15_CH2	ADC_IN3
18	-	-	-	PF4	I/O	EVENTOUT	-
19	-	-	-	PF5	I/O	EVENTOUT	-
20	14	10	10	PA4	I/O	SPI1_NSS USART1_CK USART2_CK TIM14_CH1	ADC_IN4 CKI_1

twenty one	15	11	11	PA5	I/O	SPI1_SCK	ADC_IN5
twenty two	16	12	12	PA6	I/O	SPI1_MISO TIM3_CH1 TIM1_BKIN TIM16_CH1 EVENTOUT	ADC_IN6 WKUP10
twenty three	17	13	13	PA7	I/O	SPI1_MOSI TIM3_CH2 TIM14_CH1 TIM1_CH1N TIM17_CH1 EVENTOUT MCO	ADC_IN7 WKUP11
twenty four	-	-	-	PC4	I/O	EVENTOUT	ADC_IN14
25	-	-	-	PC5	I/O	-	ADC_IN15
26	18	14	-	PB0	I/O	TIM3_CH3 TIM1_CH2N EVENTOUT	ADC_IN8
27	19	15	14	PB1	I/O	TIM3_CH4 TIM14_CH1 TIM1_CH3N	ADC_IN9
28	20	-	-	PB2	I/O	I2C1_SMBA I2C2_SMBA	-
29	twenty one	-	-	PB10	I/O	I2C1_SCL I2C2_SCL SPI2_SCK	-
30	twenty two	-	-	PB11	I/O	I2C1_SDA I2C2_SDA EVENTOUT	-
31	twenty three	16	-	VSS	I/O	Ground	
32	twenty four	17	16	VDD	I/O	Digital power supply	
33	25	-	-	PB12	I/O	SPI1_NSS SPI2_NSS TIM1_BKIN EVENTOUT I2C2_SMBA	
34	26	-	-	PB13	I/O	SPI1_SCK SPI2_SCK TIM1_CH1N I2C2_SCL	
35	27	-	-	PB14	I/O	SPI1_MISO SPI2_MISO TIM1_CH2N TIM15_CH1	

						I2C2_SDA	
36	28	-	-	PB15	I/O	SPI1_MOSI SPI2_MOSI TIM1_CH3N TIM15_CH1N TIM15_CH2	RTC_REFIN
37	-	-	-	PC6	I/O	TIM3_CH1	
38	-	-	-	PC7	I/O	TIM3_CH2	
39	-	-	-	PC8	I/O	TIM3_CH3	
40	-	-	-	PC9	I/O	TIM3_CH4	
41	29	18	-	PA8	I/O	USART1_CK TIM1_CH1 EVENTOUT MCO	-
42	30	19	17	PA9	I/O	USART1_TX TIM1_CH2 TIM15_BKIN I2C1_SCL MCO	WKUP12
43	31	20	18	PA10	I/O	USART1_RX TIM1_CH3 TIM17_BKIN I2C1_SDA I2C1_SDA	WKUP13
44	32	twenty one	-	PA11	I/O	USART1_CTS TIM1_CH4 EVENTOUT I2C2_SCL	-
45	33	twenty two	-	PA12	I/O	USART1_RTS TIM1_ETR EVENTOUT I2C2_SDA	-
46	34	twenty three	19	PA13	I/O	IR_OUT SWDIO	CKI_2
47	35	-	-	PF6	I/O	I2C1_SCL I2C2_SCL	-
48	36	-	-	PF7	I/O	I2C1_SDA I2C2_SDA	-
49	37	twenty four	20	PA14	I/O	USART1_TX USART2_TX SWCLK	CKI_3
50	38	25	-	PA15	I/O	SPI1_NSS USART1_RX USART2_RX	-

						EVENTOUT	
51	-	-	-	PC10	I/O	-	-
52	-	-	-	PC11	I/O	-	-
53	-	-	-	PC12	I/O	-	-
54	-	-	-	PD2	I/O	TIM3_ETR	-
55	39	26	-	PB3	I/O	SPI1_SCK EVENTOUT	-
56	40	27	-	PB4	I/O	SPI1_MISO TIM3_CH1 EVENTOUT BKIN	-
57	41	28	-	PB5	I/O	SPI1_MOSI I2C1_SMBA TIM16_BKIN TIM3_CH2	-
58	42	29	-	PB6	I/O	I2C1_SCL USART1_TX TIM16_CH1N	-
59	43	30	-	PB7	I/O	I2C1_SDA USART1_RX TIM17_CH1N USART4_CTS	-
60	44	31	1	Boot0	I	Boot memory selection	
61	45	-	-	PB8	I/O	I2C1_SCL TIM16_CH1	-
62	46	-	-	PB9	I/O	I2C1_SDA IR_OUT TIM17_CH1 EVENTOUT SPI2_NSS	
63	47	32	15	VSS	S	Ground	
64	48	1	16	VDD	S	Digital power supply	

Notes:

name	abbreviation	definition
pin type	S	power supply
	I	enter
	I/O	input Output
1.Unless otherwise specified, during and after reset, allI/OAll set to floating input 2.Red function pins in the above table, more pins are providedremapFunction. Please refer toGPIO Alternate Function.		

HK32F030/HK32F031/HK32F03Xseries of chips are collectively referred to asHK32F03xseries, it is moreSThe corresponding model of the brand has more functions and more flexible pin remapping function.

Function	illustrate

Wakeup	PA10/PA9/PA7/PA6 WKUP[13:10]:pass throughPWRregister enable
external system clock input	PA0/PA14/PA13/PA4 CKI_[4:1]:pass throughRCCregister enable
MCOoutput	PA7 MCOfunction: passGPIO.AFSEL[3:0] = 4'b1111 PA9 MCOFunction:HK32F030,HK32F031With this feature,Sbrand only030xChave this function
EventOut	PC[4:0] EventoutFunction: HK32F030,HK32F031With this feature,Sbrand only030have this function
USART1	PA4[4:0] USART1 CK/RX/TX/RTS/CTSFunction: HK32F030x4/HK32F030x6/HK32F031have this feature PA[15:14] USART1 RX/TXFunction: HK32F030x4/ HK32F030x6/HK32F031have this feature
USART2	PA4[4:0] USART2 CK/RX/TX/RTS/CTSFunction: HK32F030x8have this feature PA[15:14] USART2 RX/TXFunction: HK32F030x8have this feature
TIM3	PC[9:6] TIM3_CH[4:1]Function: HK32F030,HK32F031With this feature,Sbrand only030xChave this function
TIM15	PA1 TIM15_CH1NFunction: HK32F030,HK32F031With this feature,Sbrand only030xChave this function
TIM17	PB4 TIM17_BKINFunction: HK32F030,HK32F031With this feature,Sbrand only030xChave this function
SPI1/I2S1	PB[15:12] SPI1 MOSI/MISO/SCK/NSSFunction: HK32F030x4/ HK32F030x6/HK32F031have this feature PB[15:12] I2S1 SD/ MCK/CK/WSFunction: HK32F030x4/HK32F030x6/HK32F031have this feature SPIandI2Sfunctionpinis multiplexed bySPIregister to select.
SPI2/I2S2	PC2 SPI2_MISO/PC3 SPI2_MOSI/PB10 SPI2_SCK/PB9 SPI2_NSSFunction: HK32F030, HK32F031With this feature,Sbrand only030xChave this function PB[15:12] SPI2 MOSI/MISO/SCK/NSSFunction: HK32F030x8have this feature PB[15:12] I2S2 SD/MCK/CK/WSFunction: HK32F030x8have this feature SPIandI2Sfunctionpinis multiplexed bySPIregister to select.
I2C1	PF[1:0] I2C1 SCL/SDAFunction: HK32F030,HK32F031With this feature,Sbrand only030xChave this function PB2 I2C1 SMBAFunction: Pass GPIO.AFSEL[3:0] = 4'b1111 enable this function, HK32F030x4/HK32F030x6/HK32F031With this feature,SBrands do not have this feature PB[11:10] I2C1 SDA/SCLFunction: HK32F030x4/HK32F030x6/HK32F031have this feature PA[10:9] I2C1 SDA/SCLFunction: HK32F030,HK32F031With this feature,Sbrand only030x4/030x6/ 030xCseries and 031series have this function

	PF[7:6] I2C1 SDA/SCLFunction: HK32F030x4/ HK32F030x6/HK32F031have this feature
I2C2	PB2 I2C2 SMBAFunction: pass throughGPIO.AFSEL[3:0] = 4'b1111enable this function,HK32F030x8With this feature,S Brands do not have this feature PB[11:10] I2C2 SDA/SCLFunction: HK32F030x8have this feature PB12 I2C2 SMBAFunction: pass throughGPIO.AFSEL[3:0] = 4'b1111enable this function,HK32F030x8With this feature,S Brands do not have this feature PB[14:13] I2C2 SDA/SCLFunction: HK32F030have this function,Sbrand only030xChave this function PA[12:11] I2C2 SDA/SCLFunction: HK32F030have this function,Sbrand only030xChave this function PF[7:6] I2C2 SDA/SCLFunction: HK32F030x8have this feature I2C2Optionally use internalRCAs a clock source, it can stillSTOPwake up.SBrands do not have this feature.

6 Function Description

6.1 AFFunction Description

GPIOA Port Alternate Functionchoose

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF15
PA0		USART1_CTS						
		USART2_CTS						
PA1	EVENTOUT	USART1_RTS				TIM15_CH1N		
		USART2_RTS						
PA2	TIM15_CH1	USART1_TX						
		USART2_TX						
PA3	TIM15_CH2	USART1_RX						
		USART2_RX						
PA4	SPI1_NSS I2S1_WS	USART1_CK			TIM14_CH1			
		USART2_CK						
PA5	SPI1_SCK I2S1_CK							
PA6	SPI1_MISO I2S1_MCK	TIM3_CH1	TIM1_BKIN			TIM16_CH1	EVENTOUT	
PA7	SPI1_MOSI I2S1_SD	TIM3_CH2	TIM1_CH1N		TIM14_CH1	TIM17_CH1	EVENTOUT	MCO
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT				

PA9	TIM15_BKIN	USART1_TX	TIM1_CH2		I2C1_SCL	MCO		
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3		I2C1_SDA			
PA11	EVENTOUT	USART1_CTS	TIM1_CH4			I2C2_SCL		
PA12	EVENTOUT	USART1_RTS	TIM1_ETR			I2C2_SDA		
PA13	SWDIO	IR_OUT						
PA14	SWCLK	USART1_TX						
		USART2_TX						
PA15	SPI1_NSS	USART1_RX		EVENTOUT				
	I2S1_WS	USART2_RX						

GPIOB Port Alternate Functionchoose

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF15
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N					
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N					
PB2								I2C1_SMBA
								I2C2_SMBA
PB3	SPI1_SCK I2S1_CK	EVENTOUT						
PB4	SPI1_MISO I2S1_MCK	TIM3_CH1	EVENTOUT			TIM17_BKIN		
PB5	SPI1_MOSI I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA				
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N					
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N					
PB8		I2C1_SCL	TIM16_CH1					

PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT		SPI2_NSS I2S2_WS		
PB10		I2C1_SCL				SPI2_SCK I2S2_CK		
		I2C2_SCL						
PB11	EVENTOUT	I2C1_SDA						
		I2C2_SDA						
PB12	SPI1_NSS/I2S1_WS	EVENTOUT	TIM1_BKIN			TIM15_BKIN		I2C2_SMBA
	SPI2_NSS/I2S2_WS							
PB13	SPI1_SCK/I2S1_CK		TIM1_CH1N			I2C2_SCL		
	SPI2_SCK/I2S2_CK							
PB14	SPI1_MISO/I2S1_MCK	TIM15_CH1	TIM1_CH2N			I2C2_SDA		
	SPI2_MISO/I2S2_MCK							
PB15	SPI1_MOSI/I2S1_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N				
	SPI2_MOSI/I2S2_SD							

GPIOC Port Alternate Functionchoose

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT							
PC1	EVENTOUT							
PC2	EVENTOUT	SPI2_MISO/I2S2_MCK						
PC3	EVENTOUT	SPI2_MOSI/I2S2_SD						
PC4	EVENTOUT							
PC5								
PC6	TIM3_CH1							
PC7	TIM3_CH2							
PC8	TIM3_CH3							

PC9	TIM3_CH4							
PC10								
PC11								
PC12								
PC13								
PC14								
PC15								

GPIOD Port Alternate Functionchoose

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD2	TIM3_ETR							

GPIOF Port Alternate Functionchoose

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0		I2C1_SDA						
PF1		I2C1_SCL						
PF4	EVENTOUT							
PF5	EVENTOUT							
PF6		I2C1_SCL						
		I2C2_SCL						
PF7		I2C1_SDA						
		I2C2_SDA						

6.2 USARTpin mapping

USARTMultiplexing function

Group	Pin	USART1	USART2
1	PA2/PA3	only030x4/030x6/031to provide	030x8to provide
2	PA9/PA10	030x4/030x6/030x8/031can provide	Not provided
3	PA14/PA15	only030x4/030x6/031to provide	030x8to provide
4	PB6/PB7	030x4/030x6/030x8/031can provide	Not provided

6.3 I2Cpin mapping

I2CMultiplexing function

Group	Pin	I2C1	I2C2
1	PF0/PF1	030x4/030x6/030x8/031can provide	Not provided
2	PB10/PB11	only030x4/030x6/031to provide	030x8to provide
3	PB13/PB14	Not provided	030x4/030x6/030x8can provide
4	PA9/PA10	030x4/030x6/030x8/031can provide	Not provided
5	PA11/PA12	Not provided	030x4/030x6/030x8can provide
6	PF6/PF7	only030x4/030x6/031to provide	030x8to provide
7	PB6/PB7	030x4/030x6/030x8/031can provide	Not provided
8	PB8/PB9	030x4/030x6/030x8/031can provide	Not provided

6.4 SPIpin mapping

SPIMultiplexing function

Group	Pin	SPI1/I2S1	SPI2/I2S2
1	PC2/PC3/PB10/PB9	030x4/030x6/030x8can provide	Not provided
2	PA4/PA5/PA6/PA7	030x4/030x6/030x8can provide	Not provided
3	PB12/PB13/PB14/PB15	only030x4/030x6/031before you can supply	030x8to provide
4	PA15/PB3/PB4/PB5	030x4/030x6/030x8can provide	Not provided

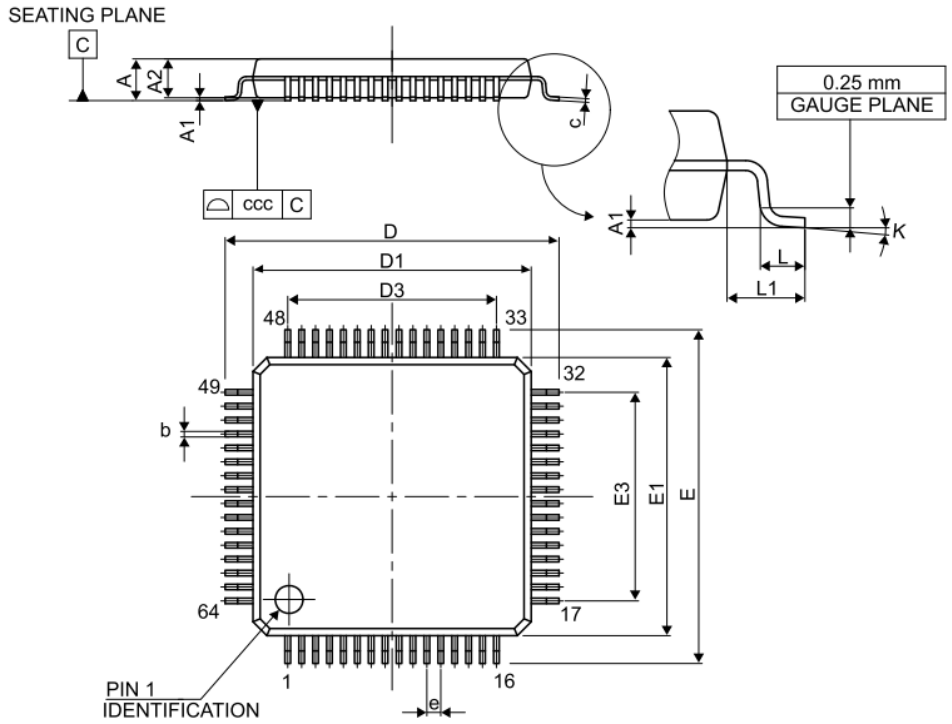
6.5 Other function mapping

GPIO Port	PMU	RCC	ADC Input	RTC
PA0	WKUP1	CKI_4	AIN0	RTC_TAMP2
PA1			AIN1	
PA2			AIN2	
PA3			AIN3	
PA4		CKI_1	AIN4	
PA5			AIN5	
PA6	WKUP10		AIN6	
PA7	WKUP11		AIN7	
PA8				
PA9	WKUP12			
PA10	WKUP13			
PA11				
PA12				
PA13		CKI_2		
PA14		CKI_3		
PA15				
PB0			AIN8	
PB1			AIN9	
PB2				
PB3				
PB4				
PB5				
PB6				
PB7				
PB8				
PB9				
PB10				
PB11				
PB12				
PB13				
PB14				
PB15		RTC_REFIN		
PC0			AIN10	
PC1			AIN11	
PC2			AIN12	
PC3			AIN13	
PC4			AIN14	
PC6				

PC7				
PC8				
PC9				
PC10				
PC11				
PC12				
PC13	WKUP2	RTC_TAMP2 RTC_TS RTC_OUT		
PC14				
PC15		LSE_CKI		
PD2				
PF0		HSE_CKI		
PF1				
PF2				
PF3				
PF4				
PF5				
PF6				
PF7				

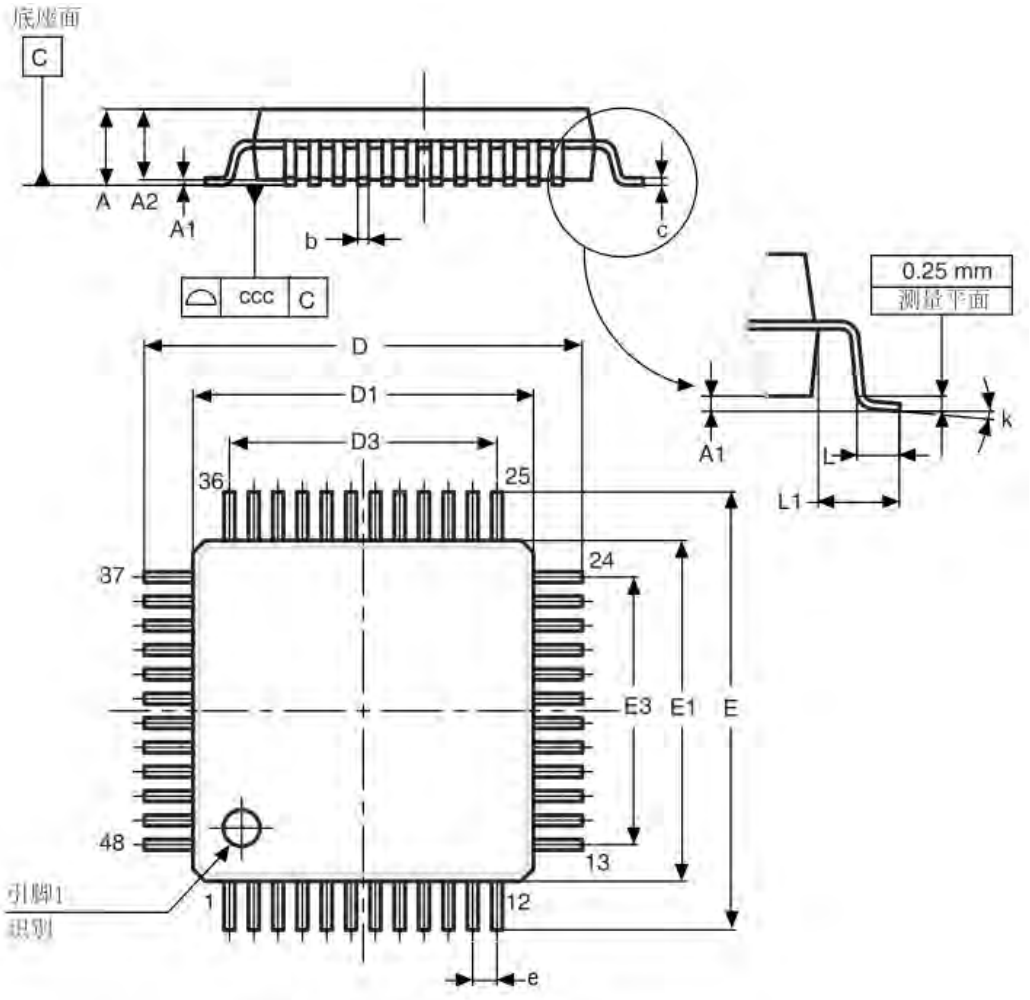
7 Package parameters

7.1 LQFP64 10x10mm, 0.5mm pitch



Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

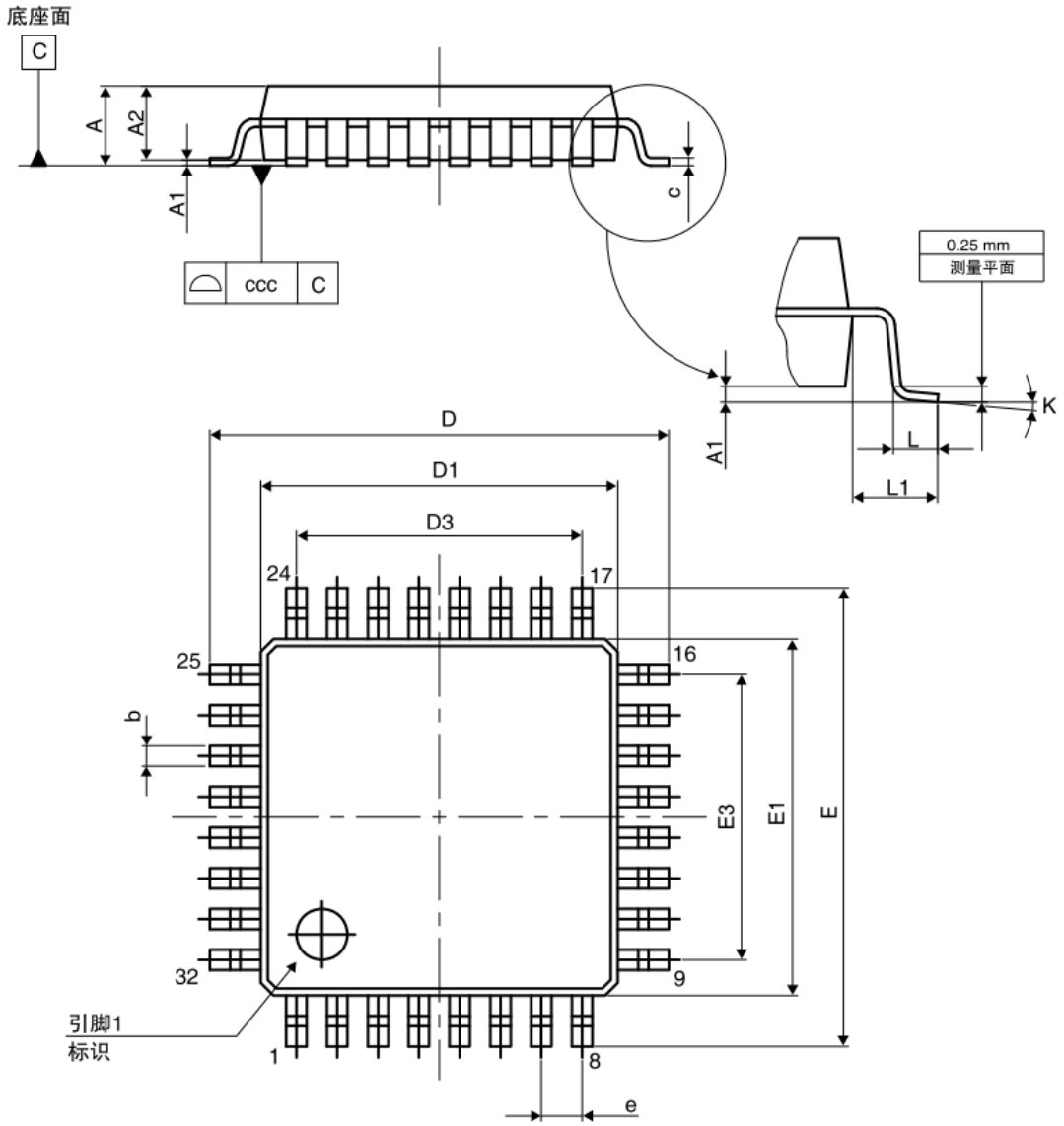
7.2 LQFP48 7x7mm,0.5mm pitch



符号	毫米			英寸(1)		
	最小值	典型值	最大值	最小值	典型值	最大值
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835

符号	毫米			英寸(1)		
	最小值	典型值	最大值	最小值	典型值	最大值
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

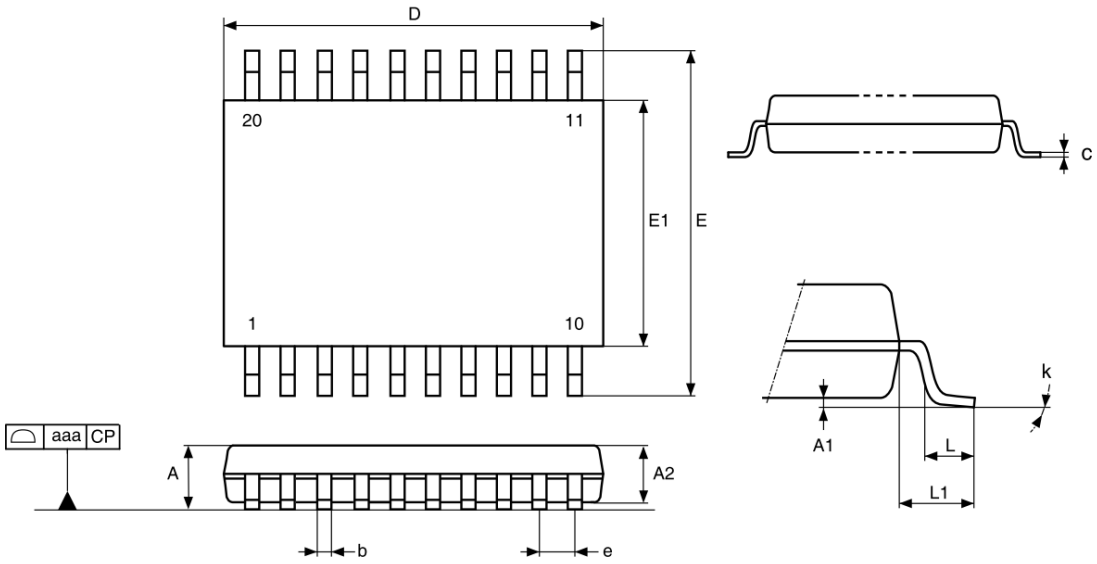
7.3 LQFP32 7x7mm,0.8mm pitch



符号	毫米			英寸(1)		
	最小值	典型值	最大值	最小值	典型值	最大值
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622

符号	毫米			英寸(1)		
	最小值	典型值	最大值	最小值	典型值	最大值
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.100	-	-	0.0039

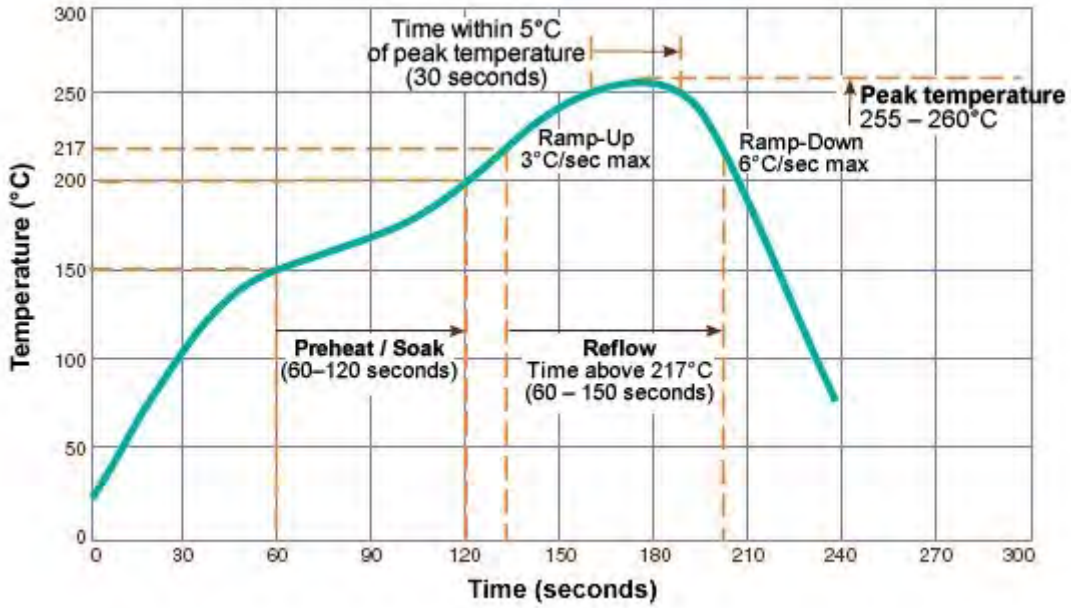
7.4 TSSOP20 0.65mm pitch



符号	毫米			英寸[1]		
	最小值	典型值	最大值	最小值	典型值	
A			1.2			0.0472
A1	0.05		0.15	0.002		0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19		0.3	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D[2]	6.4	6.5	6.6	0.252	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1[3]	4.3	4.4	4.5	0.1693	0.1732	0.1772
e		0.65			0.0256	
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
k	0.0°		8.0°	0.0°		8.0°
aaa			0.1			0.0039

8 Reflow Soldering Temperature Rise Curve

for reliableSMTwelding,HK32F030The recommended temperature rise curve of the series products is as follows:



9 abbreviation

term	Definition
RTC	real time clock
IIC	Inter-Integrated Circuit Interface
CPU	Center process unit
PLL	Phase lock loop
LDO	Low voltage drop output
RISC	Reduced Instruction-Set Computer
UART	Universal Asynchronous Receiver Transmitter
SPI	Serial peripheral interface
USB	Universal Serial Bus
GPIO	General purpose input output
CAN	Controller Area Network
I/O	Input output
ADC	Analogue to digital converter
MCU	Micro controller unit
HSE	High-speed external
HSI	High-speed internal
LSE	Low-speed external
LSI	Low-speed internal
SAR	Successive Approximation Analog-to-Digital Converter
USART	Universal Synchronous Asynchronous Receiver Transmitter
PVD	Power voltage detect
SOC	System on chip
JTAG	Joint Test Action Group
PWM	Pulse Width Modulation
DMA	Direct Memory Access
SDIO	Secure Digital Input Output
POR	Power on reset
PDR	Power down reset
CRC	Cyclic Redundancy Check
HK32F030	AirlineCortex-M0series chip
HK32F031	AirlineCortex-M0series chip
HK32F03X	AirlineCortex-M0series chip

10important hint

Without the consent of Shenzhen Hangshun Chip Technology R&D Co., Ltd., the company's product specifications shall not be modified in any form or way.

any section and subsection in the grid and data table. Shenzhen Hangshun Chip Technology R&D Co., Ltd. reserves the right to:

Modify data sheets and/or products, discontinue any product, or discontinue service without notice; customers are advised to obtain the latest version of the relevant information

information, and verify it before placing an order to ensure the timeliness and completeness of the information. All products are available upon order confirmation

are sold under the terms of the sales contract, including the scope of warranty, intellectual property rights and liability.

Shenzhen Hangshun Chip Technology R&D Co., Ltd. guarantees that during the sales period, the performance of the product is guaranteed according to the company's standard. male

The company deems it necessary to maintain this warranty and uses testing and other quality control techniques. In addition to government mandates, other instruments

No special test is necessary for the measurement table.

The customer recognizes that the design and production of the company's products do not involve life support or other dangerous activities

Or in other systems or products in the environment. A malfunctioning product can cause personal injury, property or environmental damage (collectively, high-risk

Activity). The artificial use of the company's products in high-risk activities, the company does not guarantee, and will not be responsible for customers or third parties.

responsible.

Shenzhen Hangshun Chip Technology R&D Co., Ltd. will provide the same technical support, help, advice and information as now, (Complete

Section includes design, development or debugging on purchased circuit boards or other applications). Hereby declare that for all technical support

support, marketability, or for a particular purpose, and that circuit boards and other applications may operate or function without error in the supporting technology,

The company will not make any warranty about such support technology, and will not be responsible for your use of this support service.